LESSON PLAN,SESSION-WINTER-2023-24
SWAMI VIVEKANANDA SCHOOL OF ENGG & TECH, BBSR

DISCIPLINE-ETC ENGG.	SEMISTER-3RD	NEME OF THE FACULTY-ER. SRIDHARA KUMAR RATH
SUBJECT- DE	NO OF CLASS ALLOTED/WEEK-4	SEMESTER FROM-01.08.2023 TO 30.11.2023.
WEEK	DATE	TOPICS
1ST	01.08.23	**Basics of Digital Electronic**
	04.08.23	Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system.
	05.08.23	Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system.
2ND	07.08.23	Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1's & 2's complement of Binary numbers& Subtraction using complements method
	08.08.23	Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1's & 2's complement of Binary numbers& Subtraction using complements method
	11.08.23	Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes.
	12.08.23	Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagra
3RD	14.08.23	Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagra
	18.08.23	Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagra
	19.08.23	Universal Gates& its Realisation
4TH	21.08.23	Boolean algebra, Boolean expressions, Demorgan's Theorem
	22.08.23	Represent Logic Expression: SOP & POS forms
	25.08.23	Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don't care conditions
	26.08.23	Karnaugh map (3 & 4 Variables)&Minimization of logical expressions ,don't care conditions
5TH	28.08.23	**Combinational logic circuits**
	29.08.23	Half adder, Full adder, Half Subtractor, Full Subtractor, Serial and Parallel Binary 4 bit adder
1ST	01.09.23	Half adder, Full adder, Half Subtractor, Full Subtractor, Serial and Parallel Binary 4 bit adder
	02.09.23	Half adder, Full adder, Half Subtractor, Full Subtractor, Serial and Parallel Binary 4 bit adder
2ND	04.09.23	Multiplexer (4:1), De- multiplexer (1:4), Decoder, Encoder, Digital comparator (3 Bit)
	05.09.23	Multiplexer (4:1), De- multiplexer (1:4), Decoder, Encoder, Digital comparator (3 Bit)
	08.09.23	Multiplexer (4:1), De- multiplexer (1:4), Decoder, Encoder, Digital comparator (3 Bit)
	09.09.23	Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
3RD	11.09.23	Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
	12.09.23	Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
	15.09.23	Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)

	16.09.23	Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above)
4TH	18.09.23	REVISION
	22.09.23	**Sequential logic Circuits**
	23.09.23	Principle of flip flops operation, its Types,
5TH	25.09.23	SR Flip Flop using NAND,NOR Latch (un clocked)
	26.09.23	SR Flip Flop using NAND,NOR Latch (un clocked)
	29.09.23	SR Flip Flop using NAND,NOR Latch (un clocked)
	30.09.23	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
1ST	03.10.23	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	06.10.23	CLASS TEST
	07.10.23	Clocked SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
2ND	09.10.23	Concept of Racing and how it can be avoided.
	10.10.23	Concept of Racing and how it can be avoided.
	13.10.23	Concept of Racing and how it can be avoided.
	14.10.23	REVISION
3RD	16.10.23	INTERNAL
	17.10.23	INTERNAL
	18.10.23	INTERNAL
	19.10.23	INTERNAL
4TH	21.10.23 TO 2	PUJA HOLIDAYS
5TH	30.10.23	**Registers, Memories & PLD**
	31.10.23	Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
1ST	03.11.23	Universal shift registers-Applications.
	04.11.23	Types of Counter & applications
2ND	06.11.23	Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter. Synchronous counter, Ring Counter
	07.11.23	Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
	10.11.23	Basic concept of PLD & applications
	11.11.23	**A/D and D/A Converters**
3RD	13.11.23	Necessity of A/D and D/A converters.
	14.11.23	D/A conversion using weighted resistors methods. D/A conversion using R-2R ladder (Weighted resistors) network
	17.11.23	A/D conversion using counter method.
	18.11.23	A/D conversion using Successive approximate method
4TH	20.11.23	A/D conversion using Successive approximate method
	21.11.23	**LOGIC FAMILIES**
	24.11.23	Various logic families &categories according to the IC fabrication process
	25.11.23	Various logic families &categories according to the IC fabrication process
5TH	27.11.23	Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families
	28.11.23	Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families
	29.11.23	Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR)
	30.11.23	REVISION

H. O. D. DEAN(ACADEMICS) PRINCIPAL

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